6.896 BRAINTEASER #1

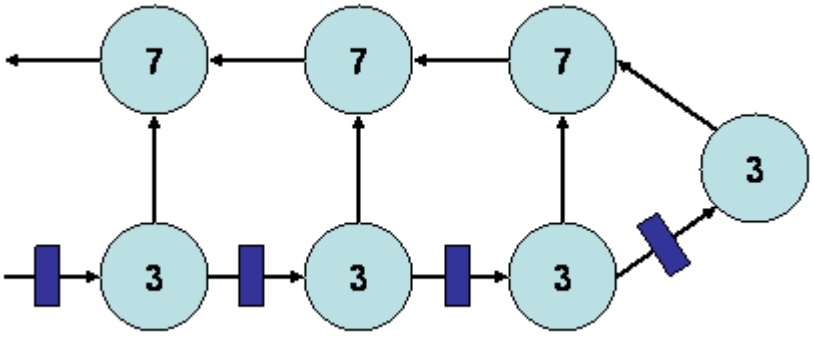

Figure 1

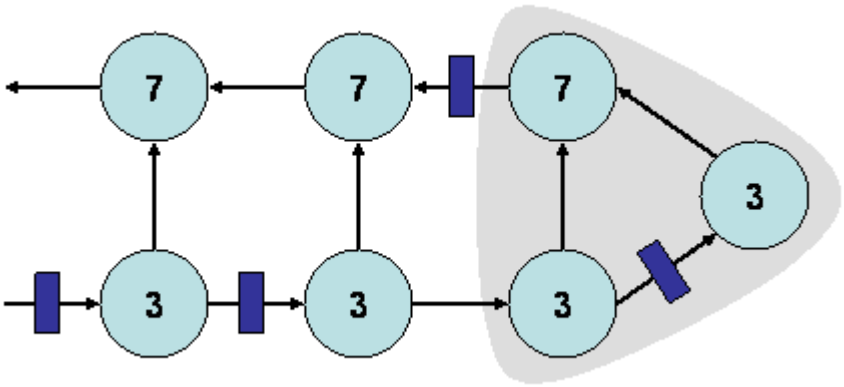

Figure 2

Figure 1 shows a sequential circuit in which circles represent combinational elements with the specified propagation delays and rectangles represent clocked registers. With each clock tick, the circuit accepts one input value and produces one output value. The clock period of the circuit is defined as the longest path of combinational rippling (accumulated propagation delay on any path between registers), which is 3+7+7+7=24.

Figure 2 shows an improved circuit with clock period 17. The new circuit has the same structure as the original one, except that registers are located in different places. The new circuit performs essentially the same function as the original one (there may be a difference in initialization), which can be seen as follows. Every input to the shaded subcircuit arrives one clock tick earlier in the new circuit compared with the old. Therefore, the computation performed by the shaded subcircuit completes one clock tick earlier in the new circuit. Thus, by delaying the output of the shaded subcircuit by one clock tick, as is done by the relocated register, the remainder of the circuit sees no difference. The new circuit, however, has a clock period of only 3+7+7=17.

What is the minimum clock period that can be obtained by relocating registers in the

circuit while still preserving its function? One restriction: to preserve the integrity of the interface, you cannot move the register on the input.