6.152/3.155
Fall 2005

Homework #1 : Solutions

① [Plummer 1.4] Estimate the resistivity of pure Si in Ω-cm at (a) room temperature (b) 77°K (c) 1000°C
Neglect the temperature dependence of carrier mobilities.

From Plummer, Eq. 1.1, we have:

$$\rho = \frac{1}{q\mu_n n + q\mu_p p}$$

where
$q = 1.6\times10^{-19}$ C
$\mu_n \sim 1500$ cm²/V·s } Values
$\mu_p \sim 500$ cm²/V·s } from text

Since we are assuming that the mobility of electrons, μ_n, and the mobility of holes, μ_p, is independent of temperature, we need to determine the concentration of electrons and holes, n and p respectively, at the given temperatures

In pure (undoped) silicon, $n=p$ due to charge neutrality. A hole and an electron are generated simultaneously when an electron breaks free from the outer orbital of a silicon atom. Keep in mind that this is not the case for doped silicon. In n-type silicon $n \gg p$ and vice versa in p-type silicon

From the law of mass action (Plummer Eq. 1.5), we have $np = n_i^2$ where n_i is dependent on temperature and can be approximated by Plummer Eq. 1.4:

$$n_i = 3.1\times10^{16}\, T^{3/2} \exp\left(\frac{-0.603\text{ eV}}{k_B T}\right) \quad [\text{cm}^{-3}] \quad (\text{for silicon})$$

Since $n=p$ for undoped Si, $n = p = n_i$

Note that T has units of Kelvin and $k_B = 1.38\times10^{-23}$ J/K
-or- $k_B = 8.625\times10^{-5}$ eV/K

(a) From the text, we are given that $n_i = 1.45\times10^{10}\,cm^{-3}$ for silicon at room temperature. We can use this value in Eq. 1.1 and solve the problem but let us see the value we obtain with Eq. 1.4.

$$n_i = 3.1\times10^{16}\,(300)^{3/2}\exp\left(\frac{-0.603}{8.625\times10^{-5}\cdot 300}\right) = 1.22\times10^{10}\ cm^{-3}$$

⇒ This value is on the same order as the value given in the text. The difference is due to round off errors

$$\therefore\ \rho = \left[1.6\times10^{-19}C\left(1500\,cm^2/V.s + 500\,cm^2/V.s\right)\left(1.22\times10^{10}\,cm^{-3}\right)\right]^{-1}$$

$$\boxed{\rho = 256\ k\Omega\cdot cm}$$

(b) @ 77°K, $n_i = 7.74\times10^{-21}\ cm^{-3} \sim 0$

We clearly see evidence of freeze out. There is a very small amount of carrier that are thermally generated.

$$\boxed{\therefore\ \rho = 4.04\times10^{35}\ \Omega\cdot cm \quad \sim \text{near infinite}}$$

⇒ essentially a perfect insulator

(c) @ 1000°C = 1273°K, $n_i = 5.80\times10^{18}\ cm^{-3}$

$$\boxed{\therefore\ \rho = 5.39\times10^{-4}\ \Omega\cdot cm}$$

Comparing this value to the resistivity of Aluminum at room temperature ($2.8\times10^{-6}\ \Omega\cdot cm$), we can see that the silicon is essentially metallic.

* In the more recent printing of Plummer, Equation 1.4 is actually: (corrected errata)

$$n_i = 3.9\times10^{16}\,T^{3/2}\exp\left(\frac{-0.603eV}{KBT}\right)\ [cm^{-3}]$$

↑

② [Plummer 1.10] - A state of the art NMOS might have a drain junction area of $0.5 \times 0.5\ \mu m^2$. Calculate junction capacitance at applied reverse bias of 2V. Assume drain is heavily doped and substrate doping is $1\times10^{16} cm^{-3}$.

Standard NMOS — Configuration where bulk and source are tied to the same potential.

Focus on the PN Junction formed by the drain and bulk.

⇒ if the junction is reverse biased, and we assume that the bulk is at ground, then the voltage at the drain is +2V

From the text, we have the following equations for a PN-junction:

$$\varphi_i = \frac{k_B T}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right) \quad \text{[Plummer Eq. 1.24]} \quad \text{and}$$

$$\frac{C}{A} = \frac{\varepsilon_{Si}}{X_d} = \left[\sqrt{\frac{q\varepsilon_{Si}}{2}\left(\frac{N_A N_D}{N_A+N_D}\right)\frac{1}{(\varphi_i \pm V)}}\right] \quad \text{[Plummer Eq. 1.25]}$$

Assuming that the drain is heavily doped, n^+ or n^{++}

$n^+ : 10^{18} cm^{-3} < n < 10^{20} cm^{-3}$; $n^{++} : 10^{20} cm^{-3} < n$

Note that assuming n^{++}, n can't exceed $10^{22} cm^{-3}$ since the semiconductor becomes degenerate and the equation for φ_i won't be entirely accurate.

If we want to find the junction capacitance, we use Plummer Eq. 1.25:

$$C = A\sqrt{\frac{q\varepsilon_{si}}{2}\left(\frac{N_A N_D}{N_A+N_D}\right)\frac{1}{(\varphi_i+V)}} \sim A\sqrt{\frac{q\varepsilon_{si}}{2}(N_A)\frac{1}{(\varphi_i+V)}}$$

(positive sign since reverse biased - increases the depletion width, lowering the capacitance)

⇒ the approximation above is valid since $N_D \gg N_A$

* The region with lighter doping has more control on the junction capacitance.

Assuming room temperature, $n_i = 1.45\times10^{10}\,cm^{-3}$, and knowing that $p \sim N_A = 1\times10^{16}\,cm^{-3}$, we can solve for φ_i for assumed concentrations of N_D.

$\frac{k_B T}{q} \sim 26mV$ @ room temperature (good value to memorize)

$$\therefore \varphi_i = \begin{cases} \sim .82V & @\ 1\times10^{18}\,cm^{-3} \\ \sim .88V & @\ 1\times10^{19}\,cm^{-3} \\ \sim .94V & @\ 1\times10^{20}\,cm^{-3} \end{cases}$$

$\sim 1.00V$ @ $1\times10^{21}\,cm^{-3}$

$\sim 1.06V$ @ $1\times10^{22}\,cm^{-3}$

—OR— assume 0.7 Volts

For the following work, I am assuming $N_D = 1\times10^{20}\,cm^{-3} \Rightarrow \varphi_i = .94V$

$\varepsilon_{si} = 11.7\varepsilon_0 \Rightarrow 11.7(8.85\times10^{-12}\,F/m) = 1.03545\times10^{-12}\,F/cm$

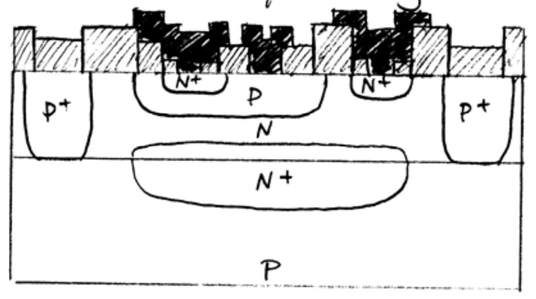
$$C = [0.5\times10^{-4}cm]^2\sqrt{\frac{q\varepsilon_{si}}{2}(1\times10^{16}cm^{-3})\frac{1}{(.94+2)}} = \boxed{4.2\times10^{-17}F}$$

(b) Compare to gate capacitance of the same area with SiO_2 thickness of 2.5nm. Assume silicon is a metal.

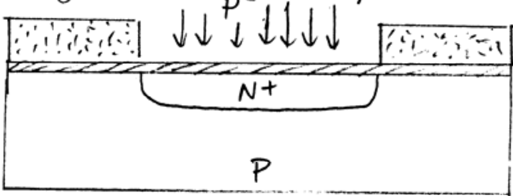
$\varepsilon_{ox} = 3.9\varepsilon_0 \Rightarrow 3.9\times8.85\times10^{-12}\,F/m = 3.4515\times10^{-11}\,F/m$

$$C = \frac{\varepsilon_{ox}A}{t_{ox}} = \frac{3.4515\times10^{-11}\frac{F}{m}(0.5\times10^{-6}m)^2}{2.5\times10^{-9}m} = \boxed{3.45\times10^{-15}F}$$

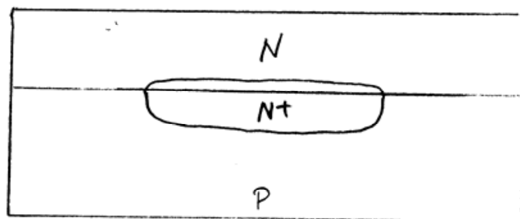
③ Cross section is a simple bipolar transistor. Design a plausible process flow. You don't have to include any quantitative process parameters. Answer should be sketches, explaining for each step and order chosen.



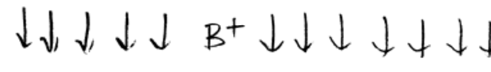
⇒ There are many correct answers to this problem. The point of this exercise is to make you think about a process flow and to keep track of process history.

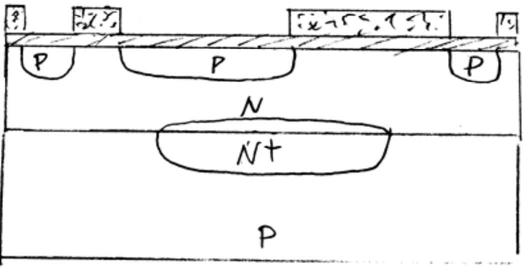


• Start with p-type wafer, grow thin oxide by dry oxidation (to prevent channeling), coat and pattern resist, then implant phosphor ions to form N^+ region that is "buried".

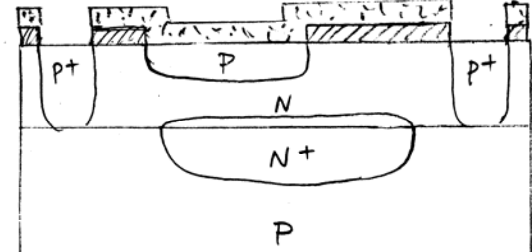


• Strip resist with O_2 plasma or chemical wet etch, strip oxide with plasma or buffered oxide etch (dilute HF), anneal to repair lattice from implant. Grow in-situ n-type epitaxial layer.

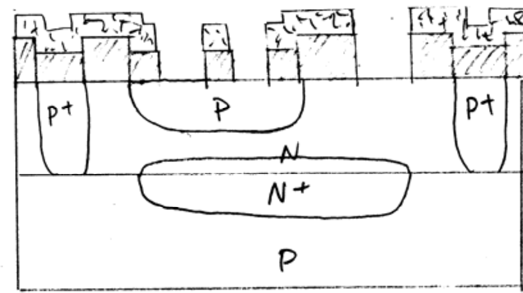




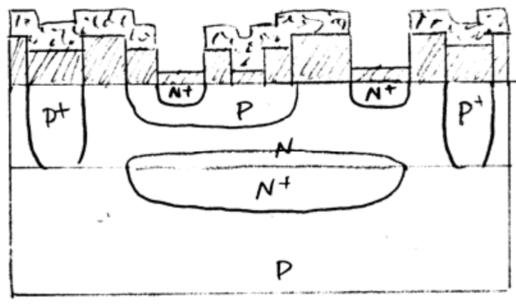
• Grow thin oxide with thermal oxidation, coat and pattern resist, then implant boron ions to form p well and parts of the p^+ isolation regions.



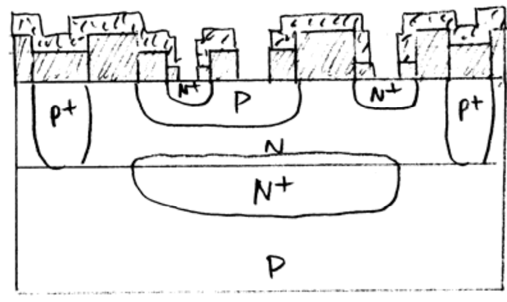
- Dry or wet etch oxide using previous resist as mask. Strip the resist with O_2 plasma or chemical etch. Coat and pattern a new layer of resist. Implant more boron ions to complete p^+ isolation regions. Note that there is no oxide, permitting ions to travel deep into the epitaxial layer.



- Strip resist, anneal, deposit oxide using chemical vapor deposition (CVD). Coat and pattern resist. Use dry or wet etch to pattern the oxide for the N+ implants and contacts.



- Strip resist, grow thin layer of thermal oxide. Coat and pattern new resist layer for Phosphor ion implant to form N+ regions. The thermal oxide is to keep the implants shallow.



- Strip old resist, anneal, coat + pattern new resist for oxide etch to form contacts to the Base, Emitter, and Collector of the BJT. Etch the oxide to expose contact regions.

- To obtain the final cross section, strip the resist. Spin and pattern new resist for metallization. Sputter metal; strip new resist, and anneal the wafer so metal forms a denser film.