

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.976
High Speed Communication Circuits and Systems
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Homework #1: *S*-parameters, transformers, ISI, and eye diagrams

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Reading: Chapters 4-6 of Thomas H. Lee's book, CppSim manual, Hspice toolbox manual.

1. Consider the high speed trace and its associated two-port model shown in Figure 1. In the model, the transmission line corresponds to the RF connector and PCB trace (both assumed to be ideal), C_1 is the capacitance of the package pin to the package substrate and adjoining pins, L_1 is the bondwire inductance, C_2 is the on-chip pad capacitance, and R_L is the on-chip termination resistor. For all calculations to follow, it is assumed that the source driving impedance is precisely matched to the transmission line characteristic impedance, R_o .

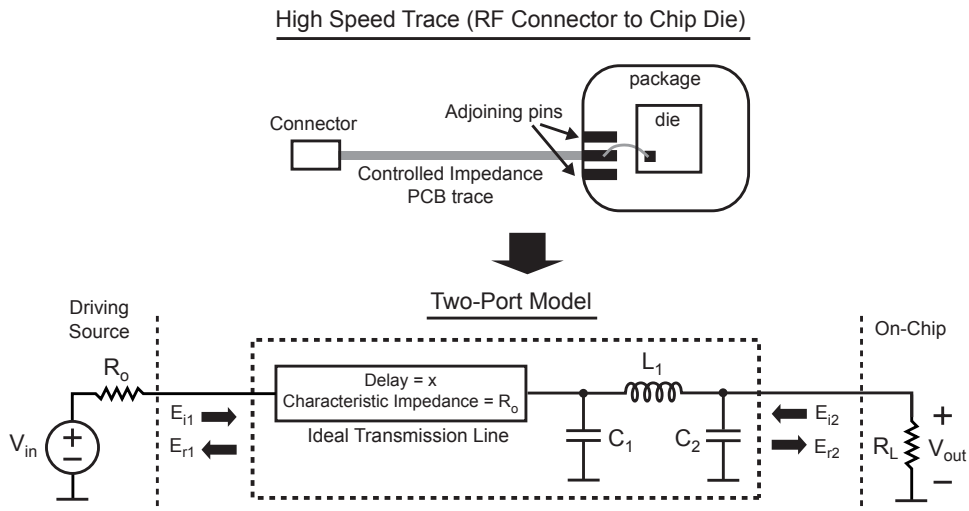


Figure 1: Example high speed trace and associated 2-port model.

Calculate S_{11} and S_{21} for each of the following cases:

- (a) $R_o = 50$ Ohms, $x = 0$ ps, $C_1 = 0.0$ pF, $L_1 = 0$ nH, $C_2 = 0$ pF, $R_L = 55$ Ohms
- (b) $R_o = 50$ Ohms, $x = 0$ ps, $C_1 = 0.0$ pF, $L_1 = 0$ nH, $C_2 = 1$ pF, $R_L = 55$ Ohms
- (c) $R_o = 50$ Ohms, $x = 100$ ps, $C_1 = 0.0$ pF, $L_1 = 0$ nH, $C_2 = 1$ pF, $R_L = 55$ Ohms

- (d) $R_o = Z_o$, $x = \text{delay}$, $C_1 = C_1$, $L_1 = L_1$, $C_2 = C_2$, $R_L = Z_L$
- (e) Using CppSim on Athena, verify part(c) by simulating the impulse response of the system using the hw1_1e.i ($C_1 = 0.0$ pF) and hw1_1e.ii ($C_1 = 1.0$ pF) cells within the CppExamples Cadence library and its associated test.par files in the UNIX directory $\sim/\text{CppSim}/\text{SimRuns}/\text{CppExamples}$. Based on the simulation results, plot the magnitude and phase of $S_{11}(f)$ and $S_{21}(f)$ for both cases.

2. The following problem is taken from problem 2 of Chapter 4 from Thomas Lee's book. Suppose we wish to deliver 1 Watt of power into a 50 Ohm load at 1 GHz, but are constrained to using a power amplifier that has a peak-to-peak sinusoidal voltage of only 3 V due to transistor breakdown issues. Design the following matching networks to allow that 1 W to be delivered. Use lowpass versions in all cases, and assume that all reactive elements are ideal.

- (a) L-match
- (b) π -match ($Q = 10$)
- (c) T-match ($Q = 10$)
- (d) Tapped capacitor ($Q = 10$)
- (e) If the maximum allowable on-chip capacitance is 200 pF and the maximum allowable on-chip inductance is 20 nH, are any of your designs amenable to a fully integrated implementation? If so, which one(s)?

3. Simulate the transformer networks computed in Problem 2 in Hspice on Athena. Be sure to use Cadence for design entry as specified in the documents handed out in class. Assume that the source driving impedance is a resistor that matches the nominal input impedance of the transformer at 1 GHz. Adjust the input source voltage such that 3 V peak-to-peak exist at the inputs of the transformer networks.

Based on the Hspice results, compute and plot S_{21} of each transformer network (from transformer input to output) across the frequency range of 900 MHz to 1.1 GHz. Comment on the differences between the performance of each transformer. (Note: you should reference the input as the signal source rather than the input to the transformer - why?)

4. Now consider the high speed trace and its associated two-port model shown in Figure 2, which is similar to that examined in Problem 1. In this case, we will relate the transmission line parameters to physical PCB characteristics, simulate the system, and observe eye diagrams of high speed data being sent across the trace. For all parts of this problem, assume that C_1 and L_1 are zero unless otherwise noted.

- (a) Assuming that the PCB trace is a 0.5 ounce Microstrip whose dielectric has $\epsilon_r = 4.4$ and a height of 10 mils, use the web-based tool at <http://www.emclab.umr.edu/pcbtlc> to perform the following calculations (note: you must use Internet Explorer).

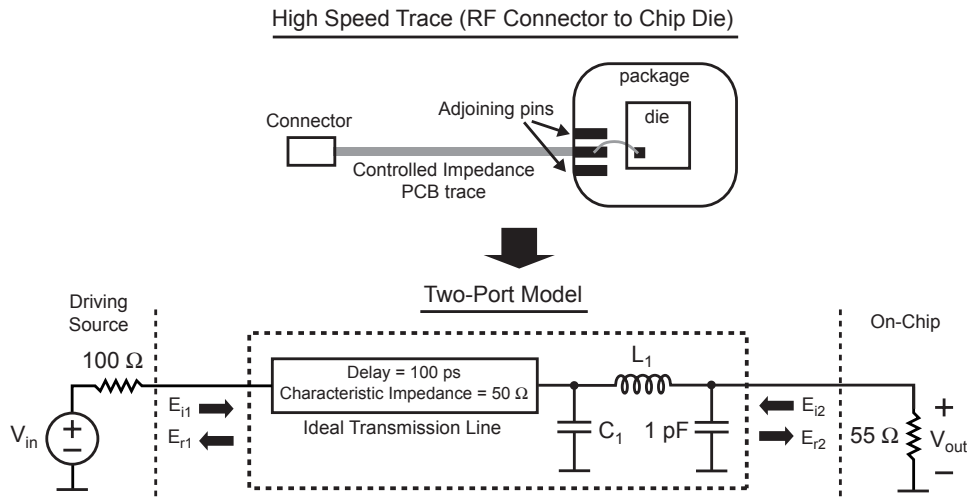


Figure 2: Example high speed trace and associated 2-port model.

- i. Determine the required width of the PCB trace to achieve 50 Ohms characteristic impedance.
 - ii. Calculate how long the trace must be to match the assumed propagation delay of 100 ps.
- (b) Using CppSim on Athena, simulate the step response of the system using the hw1_4b cell within the CppExamples Cadence library and its associated test.par file in the UNIX directory \sim /CppSim/SimRuns/CppExamples.
- i. Label the cause of the first 5 steps in the overall step response.
 - ii. Why does the cap cause its respective reflection to go negative?
- (c) Using CppSim on Athena, simulate the response of the system to an input data sequence using the hw1_4c cell within the CppExamples Cadence library and its associated test.par file in the UNIX directory \sim /CppSim/SimRuns/CppExamples.
- i. Plot the eye diagram (spanning two data periods) corresponding to V_{out} for a data rate of 1 Gb/s. Mark the ideal sampling point assuming a hard-decision detector is used, and comment on the quality of the eye.
 - ii. Plot the eye diagram (spanning two data periods) corresponding to V_{out} for a data rate of 10 Gb/s. Mark the ideal sampling point assuming a hard-decision detector is used, and comment on the quality of the eye.
- (d) Create a new module to support the load having C_1 and L_1 with nonzero values. Note that the symbol is already provided as trline_load2 in the Cadence library CppModules as well as a template of the module function in modules.par under the same name. So, for this part of the homework, simply turn in the appropriate code for module trline_load2 in modules.par.