Code No: 5455AG

R17

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, January - 2018

DIGITAL SYSTEM DESIGN

(Embedded Systems)

Time: 3hrs **Max.Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

5 × 5 Marks = 25

1.a) What are the capabilities and limitations of a Finite state machine. [5]
b) Explain the difference between PLA and PAL with advantages of both. [5]
c) Consider a combinational circuit Z=A+BC, draw the equivalent SM charts for the given combinational circuits. [5]
d) Write a short note on multiple stuck at fault models. [5]
e) Draw the architecture of Built in self test and explain its operation. [5]

PART - B

5 × 10 Marks = 50

2.a) Explain the procedure of state minimization using merger graph and merger table.
b) Explain about races and hazards. [6+4]

OR

3.a) Discuss about completely and incompletely specified sequential machines.
b) What is a sequential network? With a neat sketch explain about Moore model and Mealy model sequential networks. [5+5]

4. Explain the parallel binary divider and also the state diagram of a divider control circuit. [10]

OR

5.a) Design a data path and controller logic for an 8-bit serial Adder circuit. Synthesize the controller using one-hot method.
b) Design a 3-bit ripple-carry adder using an appropriate PLA with feedback. Specify the PLA size in terms of inputs, total outputs, outputs that feedback to the AND plane of the PLA, and product lines needed for the design. [5+5]

6. Draw an ASM chart to design control logic of a binary multiplier. Realize the same using MUX, decoder and D - flip flops. [10]

OR

7. Draw the SM chat for Dice game and also implement using PLA and D flip flop. [10]

8. Explain the terms (a) Fault diagnosis (b) Fault detection (c) Test generation. [10]

OR

9.a) Explain the fault equivalence and fault location in combinational circuits.

b) Explain the path sensitization method with an example. [5+5]

10. Classify the fault detection experiments for the sequential circuits with examples. [10]

OR

11.a) What is a synchronizing uncertainty vector? And what are the termination rules to obtain synchronizing tree.

b) What is the need for fault diagnosis? [5+5]

---ooOoo---