Code No: 54021 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, November/December - 2015

PULSE AND DIGITAL CIRCUITS

(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

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1.a) Show that a high pass circuit with small time constant acts as a differentiator.

b) A square wave whose peak to peak amplitude is 2V extends ±with respect to ground. The duration of the positive section is 0.1s and that of the negative section is 0.2s. If this waveform is impressed upon an RC integrating circuit whose time constant is 0.2s? What is the steady state maximum and minimum value of the output waveform? [7+8]

2.a) Explain how a sine wave is converted in to a square wave using a clipping circuit.

b) State and prove the clamping circuit theorem. [7+8]

3.a) Discuss the switching times of a junction diode in detail.

b) Explain how transistor at as a switch. [8+7]

4.a) With the help of a neat circuit diagram and waveform explain the working of a collector coupled monostable multivibrator.

b) Design a Schmitt trigger circuit for the following specifications: UTP=8V, LTP=5V, V_{CC}=15 V, I_C(sat)=2mA h_{FE}(min)=25. [7+8]

5.a) Draw a transistor current sweep circuit and explain how to generate a linearly varying current waveform.

b) Find the component values of a bootstrap sweep generator. Given V_{CC}=18 V, I_C(sat)=2mA h_{FE}(min)=30. Assume the necessary values. [7+8]

6.a) Discuss the applications of sampling sate in detail.

b) Draw a bidirectional sampling gate and derive equation for control voltages (V_c and V_n). [7+8]

7.a) How does the sync signal affect the frequency of operation of a sweep generator? Discuss the frequency division by a factor of 2 in a sweep generator.

b) What is the condition to meet for pulse synchronization? Compare sine wave synchronization with pulse synchronization. [8+7]

8.a) Draw a TTL two input NAND gate and verify the truth table.

b) Draw the AND, OR and NOT gates using diode and verify the truth table. [8+7]

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