Code No: 5157D

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech I Semester Examinations, October - 2015
CPLD AND FPGA ARCHITECTURES AND APPLICATIONS
(VLSI System Design/VLSI Design)

Time: 3hrs **Max.Marks:60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 Marks = 20

1.a) Explain the PAL Design with an example. [4]
b) Discuss about features of FPGAs. [4]
c) Briefly explain about the state assignment for FPGA. [4]
d) Explain about the the FPGA Design Dichotomy. [4]
e) Briefly explain how you design an 8 bit counter using 8 D Flip Flops. [4]

PART - B

5 × 8 Marks = 40

2. Discuss about the features of AMD's – CPLD devices in detail. [8]

OR

3. Explain about Cypress Flash 370 device technology and also explain about the merits and demerits of the technology. [8]

4. Explain about the technology mapping for FPGA's. [8]

OR

5. Explain the ACT 2 and ACT 3 FPGA architectures with neat diagrams. [8]

6.a) Explain the properties of Petrinetes.
b) Explain the traffic light controller design using Petrinetes notation. [4+4]

OR

7.a) Explain Basic concepts of Petrinetes for state machines.
b) Explain the application of the one Hot method to a serial 2's complement. [4+4]

8. Explain about front end digital design tools for FPGAs and ASICs in detail. [8]

OR

9. Explain in detail about Design process flow using ASICs. [8]

10. Give the design flow for Parallel Controllers and Parallel Adders using Mentor Graphics EDA tool. [8]

OR

11. Design a Parallel Adder unit with a carry look ahead principle. [8]

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