Code No: 5157C

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech I Semester Examinations, October - 2015

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

(VLSI System Design/VLSI Design)

Time: 3hrs **Max.Marks: 60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 Marks = 20

1.a) Explain about Channel Length Modulation. [4]

b) What are the advantages of band gap voltage reference circuit compared to other reference circuits? [4]

c) Give the advantages of Gate Drain Connected loads over Current Sources Loads. [4]

d) Explain about Cascode Operational Amplifiers. [4]

e) Draw the circuit diagram of Source Cross Coupled Pair Differential Amplifier. [4]

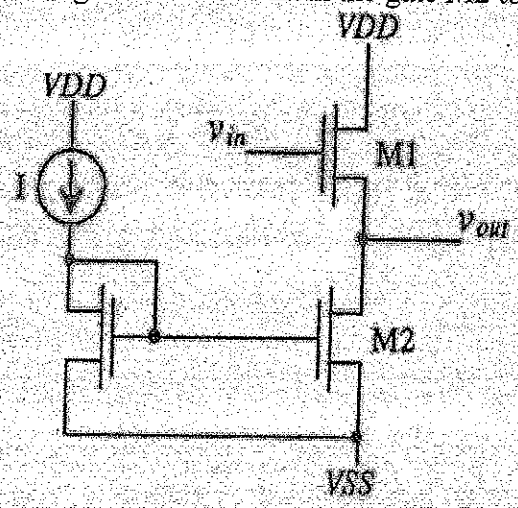
PART - B

5 × 8 Marks = 40

2. Derive the expression for threshold voltage of a MOS transistor and explain the significance of different parameters present in this equation. [8]

OR

3. For the following figure:
a) What is the small-signal resistance looking into the source of M1 and the drain of M2?
b) What is the small signal resistance from the gate M2 to the ground? [4+4]



4. Design a current sink using double cascaded current mirror with $V_{dd} = -V_{ss} = 2,5$ to a sink current of 10μA. [8]

OR

5. Design a 5μA current source using diode referenced self biasing circuit. Assume required SPICE parameters. [8]

6. Draw the circuit for differential amplifier with current source load and explain its operation. [8]

OR

7. Determine the values of +ve and –ve CMR and CMRR in the case of a differential amplifier, given for M6 with usual notation, W6 = 25 μ, L6 = 5 μ. ISS = 25 μA. Assume reasonable values of other data required if any. [8]

8. Explain about Power- Supply Rejection Ratio of Two-Stage Op Amplifiers. [8]

OR

9. Explain the Design of CMOS Op Amplifiers. [8]

10. Explain how the comparator is characterized by DC performance and transient response. [8]

OR

11. Write short notes on clocked comparator. [8]

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