Code No: R09221002 | R09 | SET-1

B.Tech II Year - II Semester Examinations, April-May, 2012
STRUCTURED DIGITAL SYSTEM DESIGN
(Common to ECC, EIE, ICE)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Given the following Truth Table:

BIF	KZ	SIB
0	0	0
0	1	1
1	0	0
1	1	1

Interpret this table and write a logic statement using the words IF, AND, OR, ASSERTED and NOT-ASSERTED.

b) Design an Excess-3 to Decimal code converter. [9+6]

2.a) Draw the schematic diagram of a tri-state buffer and explain its operation.

b) Determine the maximum number of open collector outputs (TTL) that can be tied to a single bus wire which drives 10 other inputs (TTL). Find both n and the value of R_{pullup}

c) With illustration, explain the propagation delay through an inverter. [5+5+5]

3.a) What is a sequential circuit? Distinguish it from combinational circuits.

b) Convert the RS Flip-Flop to
i) D-Flip Flop ii) T Flip-Flop.

c) Compare Mealy and Moore Machines. [4+6+5]

4.a) Discuss the steps involved in the analysis of sequential circuits.

b) What is an equivalent state? How is it used in State reduction?

c) With a suitable example, explain the design of a next state decoder. [4+4+7]

5.a) Design a 3-bit modulo 6 unit distance counter with an Asynchronous Clear.

b) Design a 3-bit universal shift register using JK flip flop to perform the following operations:
i) No Change ii) Shift right operation
iii) Shift Left operation iv) Parallel loading. [7+8]

6.a) Explain the Multi –Input System Controller design phases.

b) Illustrate the possible fault caused by an asynchronous input X changing just to the minimum set-up time limits of the D Flip-Flop. [7+8]

7.a) Draw the flow diagram for a prototype pop vending machine control system.

b) What is Functional Partitioning? Explain. [8+7]

8.a) With block diagrams explain
i) Direct addressed multiplexer configuration
ii) Indirect-Addressed multiplexer configuration.

b) With schematic diagram, explain 82S100 FPLA architecture. [7+8]

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Code No: R09221002 | R09 | SET-2

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STRUCTURED DIGITAL SYSTEM DESIGN
(Common to ECC, EIE, ICE)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) What are the advantages of digital systems?
b) Convert the number $(0.875)_{10}$ into its:
i) Binary ii) trinary iii) quinary
iv) Octal equivalents using the multiplication method.
c) Design a Carry Look-ahead adder and explain its operation. [4+4+7]

2.a) Compare Open collector and Tristate output devices.
b) Explain the practical aspects of Wired Logic and Bus oriented structures.
c) Define
i) Fan-in ii) Fan-out
iii) Propagation Delay iv) Noise Margin. [4+5+6]

3.a) Explain the need for sequential machines.
b) Design any two oscillator circuits suitable for digital system clock.
c) What is a race around condition? How is it avoided? Explain. [4+6+5]

4.a) The state equations and output equation of a sequential circuit are:
J_A= (B'C+B'X); K_A=B; J_B= (AB'+B'C); K_B=B; J_C=A'C; K_C= (B+X'),
Output = ABCX (Where X is the external input). Realize the circuit.
b) With a suitable example, explain the partitioning procedure for state minimization. [7+8]

5.a) Design a 3-bit modulo 6 unit distance counter with a Synchronous Clear.
b) Design a 4-bit parallel-in serial-out shift register and explain its operation. [8+7]

6.a) Explain the steps involved in the controller design phase.
b) Explain the first cut flow diagram for a 2's complement system.
c) How to specify the system controller states using MDS diagram. [5+5+5]

7.a) Explain the process of synchronizing two systems.
b) Write a short note on Hand Shake.
c) Explain the sequential machine with an
i) Output holding register and asynchronous input holding register
ii) Asynchronous SET/RESET register. [4+4+7]

8.a) Discuss in detail about the application of MSI Multiplexers in System controller.
b) Design a four-bit BCD to Excess-3 code converter and implement it using a (4×4) ROM. [8+7]

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Code No: R09221002 | R09 | SET-3

B.Tech II Year - II Semester Examinations, April-May, 2012
STRUCTURED DIGITAL SYSTEM DESIGN
(Common to ECC, EIE, ICE)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Define mnemonic and polarized mnemonic.
b) Implement the following Boolean function using 8-to-1 multiplexer.
F(A,B,C,D)= ∑m(0,5,6,13,14)
c) Reduce the following Boolean expression using the theorems and identities
$F = A\bar{B} + C\bar{D}B + \bar{A}C\bar{D}$ [3+8+4]

2.a) Draw schematic diagram for tri-state buffer and explain the its operation.
b) What are the practical aspects considered in designing the combinational circuits?
c) Compare the open-collector and tri-state bus system. [6+3+6]

3.a) Draw a timing diagram and illustrate SETUP time and HOLDING time. Give a qualitative description of each and how these specifications relate the hardware of the Flip-Flop.
b) Using timing diagram, analyze the D-Latch Flip-flop. Include propagation Delay in your analysis. [7+8]

4.a) Using the state diagram make state assignment for the given state diagram as shown in Fig-1.
b) Derive the next state maps for the state assignment made from the above obtained state assignment. [8+7]

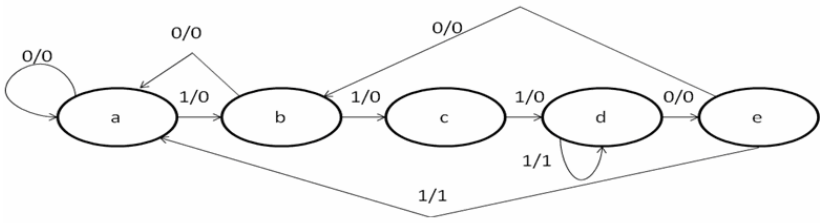

Fig-1

5.a) Design a twisted ring counter which will provide the following waveform shown in Fig-2. Make certain the counter is self-correcting.

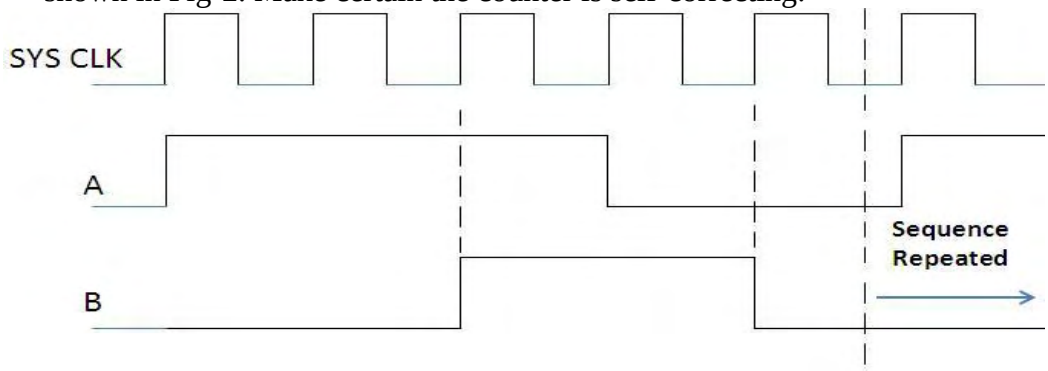

Fig-2

b) Design an odd length (modulo 7) ring counter which is initialized or reset to state 7 (111). [8+7]

6.a) Explain the Multi –Input System Controller design phases.

b) Illustrate the possible fault caused by an asynchronous input X changing just to the minimum set-up time limits of the D Flip-Flop. [7+8]

7. Design steps for the design of the controller and system for a high speed UART (Universal Asynchronous Receiver and Transmitter) able to send and receive serial data at a 1MHz rate. [15]

8. Implement the following controller using the indirect addressed multiplexer. The controller and system will add two four-bit unsigned numbers ($B_3B_2B_1B_0$ and $A_3A_2A_1A_0$) which are stored in two separate four-bit PIPO's. [15]

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Code No: R09221002 | R09 | SET-4

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Time: 3 hours **Max. Marks: 75**

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1.a) Define truth-table. What are the uses of truth tables?

b) Implement the following Boolean function using one 74154 IC (4-to-16) decoder with low asserted outputs

F(A,B,C,D)= ∑m(1,4,6,8,11,13,14)

c) Implement the following Boolean function with NOR gates

$F = C + AB + AD(B + \overline{C})$

[2+8+5]

2.a) Implement F(L) and F(H) with an A-O-I device

C \ AB				
	0	1	1	1
	0	0	0	1

where F(L) and F(H) are the functions obtained from minterm and maxterm expressions of the above K-Map respectively.

b) Define fan-out, fan-in, standard load and propagation delay. [8+7]

3.a) Define the following terms:

i) Release time ii) Setup time

iii) Transition time iv) Recovery time.

b) Using timing diagram, analyze the T Flip-flop. Include propagation delay in your analysis, illustrating the undesirable mode of operation (oscillation or hang) in it. [8+7]

4. Design a block diagram and a state diagram for a circuit which samples (with system CLK) an input line [x=1(L)]. This system is to give an indicator (SEQDET(H)) each time the three-bit sequence 110 is detected in a continuous data stream. [15]

5.a) Using universal shift register such as 74194 IC (four-bit multi-mode) design a self-correcting modulo ring counter.

b) A stepper motor drive circuit requires the following waveforms shown in Fig.1 (four signal lines) as inputs. Design a special sequence generator which will provide the necessary signals for this stepper motor drive. [7+8]

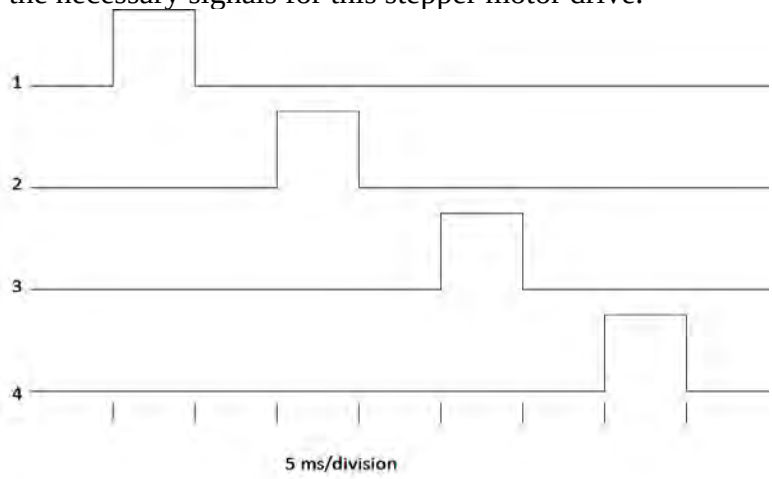

Fig. 1

6. Design a square wave duty cycle discriminator system controlled by a system controller. This system is to measure the time difference between alternate low and high portions of a low frequency quasi square wave signal (0.1 to 100Hz). [15]

7. Design a four-way traffic light controller, one that will handle traffic flow at high rates in any directions. Associate a left turn with all 4 directions as well as a pedestrian cross wall switch. [15]

8.a) Write short notes on Configurable memories.

b) Implement the following expression with PLA

$$F = \overline{A}\,\overline{B} + B\,C + \overline{B}\,\overline{C}$$ [7+8]

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