R09

Code No: C6106, C0608, C7702, C6802, C5702, C6506

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH I SEMESTER EXAMINATIONS APRIL/MAY-2012
CPLD & FPGA ARCHITECTURES AND APPLICATIONS
(COMMON TO COMMUNICATION SYSTEMS, DIGITAL SYSTEMS & COMPUTER ELECTRONICS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI&EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN, WIRELESS & MOBILE COMMUNICATIONS)

Time: 3hours **Max.Marks:60**

Answer any five questions
All questions carry equal marks
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1.a) Explain the PLA design for the fallowing
f=x'y'z+x'yz+xyz+xy'z' .
b) Explain speed performance and system programming.

2. Consider any logic block and explain routing architecture.

3. Explain the design flow technology mapping for FPGA's.

4. Explain state machine chart using micro programming linked state machine.

5. Explain hot state machine with an example.

6. Explain the front end and dsign tools for FPGA.

7. Explain the design flow using FPGA's.

8. Write short notes on the following
i) Design of parallel adder cell.
ii) Sequential circuit.
iii) Parallel controllers.

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