R09

Code No: C7704, C6804, C5704

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH I - SEMESTER EXAMINATIONS, APRIL/MAY-2012
ALGORITHMS FOR VLSI DESIGN AUTOMATION
(COMMON TO EMBEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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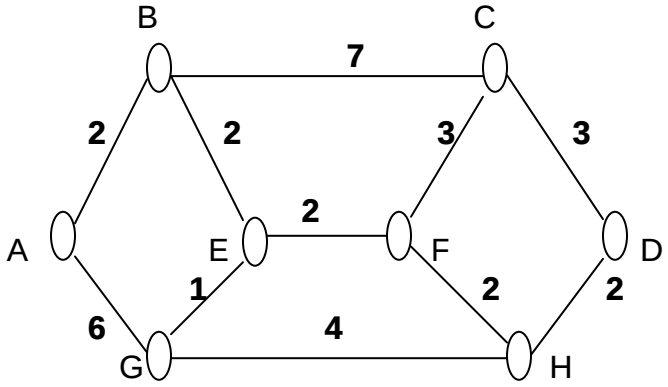
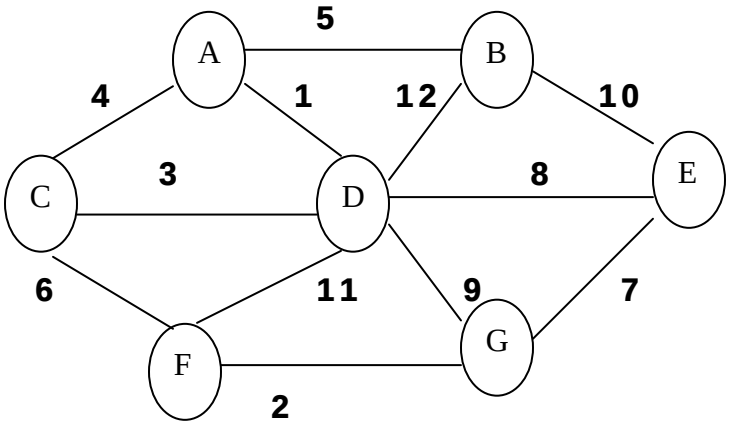
1. Find the Shortest path from the node "B" to "D" in the following graph, using Dijkstra's Algorithm. Explain the procedure of finding the required.



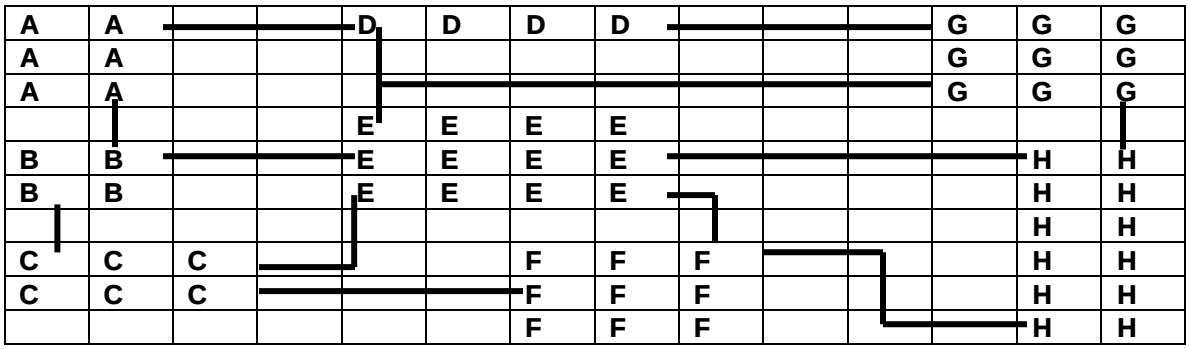
2. Find the Spanning tree for the following graph using Prim's algorithm. Explain the procedure.



3. Explain
   a) Genetic Algorithm
   b) Local Search methods

Contd…..2

4. Explain Horizontal Virtual Grid Compaction algorithm and apply the algorithm to the given layout and give the compacted layout.



In the above layout, the cell "A" is a 3x2 grid. The same applies for the remaining. The bold lines represent the connection between various cells.

5. Explain Maze Running Algorithm to find the shortest path between source and Target in a grid, and apply the algorithm to find the shortest path for the given Grid.

2	1	2	3	4	5
1	S	1	X	5	6
2	1	2	X	6	7
X	X	3	4	5	6
6	5	4	5	6	7
7	6	X	X	X	8
8	7	X		10	9
9	8	9	10		10
10	9	T			

Each integer represents the cost and S &T are source and Target respectively and "X" represents obstacle.

6. Explain about various Binary Decision Diagrams with an example.

7. Explain about the Physical Design Cycle for FPGAs.

8. Write about various MCM routing Algorithms.

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