Code No: 57035 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech IV Year I Semester Examinations, February/March -2016

VLSI DESIGN

(Common to ECE, EIE, IT)

Time: 3 Hours **Max. Marks: 75**

Answer any Five Questions

All Questions Carry Equal Marks

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1.a) Present the n-MOS fabrication process with the help of neat sketches.
b) Compare Bipolar and CMOS Technologies. [8+7]

2.a) Draw and explain different Bi-COMS Inverter circuits.
b) A PMOS transistor is operated in the triode region with the following parameters:
$V_{gs} = -4.5V$;
$V_{tp} = -1V$;
$V_{ds} = -2.2V$;
$W/L = 95$;
$\mu C_{ox} = 95\ \mu A/V^2$
Find the drain current and drain source resistance. [10+5]

3.a) Design a Stick diagram and Layout diagram for n-MOS Inverter.
b) Explain λ-based Design Rules. [8+7]

4.a) Explain the model for derivation of Time Delay.
b) Why D-Latch is called level sensitive latch.
c) Explain the problems of driving large capacitive loads? How such loads can be driven. [5+5+5]

5.a) Design briefly n-bit parallel adder and n-bit subtractor.
b) Discuss about Serial Multipliers. [10+5]

6.a) What is DRAM? How it differs from SRAM.
b) Write a brief notes on Content Addressable Memory.
c) Draw and explain one-cell of SRAM. [5+5+5]

7.a) Explain Architecture of CPLD.
b) Write the Comparison between PLA, PAL, CPLD and FPGA. [8+7]

8.a) Give the merits of Boundary Scan Check.
b) Write a note on System-Level Test Techniques.
c) What are the design strategies for test? [5+5+5]

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