Code No: 56029 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year II Semester Examinations, May - 2016
VLSI DESIGN
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Explain the following terms related to IC production process
i) Diffusion
ii) Metallization
iii) Encapsulation
b) Explain the fabrication process of NMOS with suitable diagrams. [8+7]

2.a) Draw and explain different pull-up circuits.
b) Draw and explain circuit diagram, VTC and current characteristics of CMOS inverter. [6+9]

3.a) With each step explain VLSI Design Flow in detail.
b) Draw the layout diagram of 3 input CMOS NAND gate. [8+7]

4.a) Explain the effect of cascaded inverters as drivers.
b) What are the different choices between layers to meet user specifications? [8+7]

5.a) Draw and explain the function of 4 bit ripple carry adder.
b) Draw the circuit diagram Zero/one detector and explain its operation. [7+8]

6.a) Draw basic DRAM Cell and explain its operation.
b) Draw 4-bit ROM and explain its operation. [7+8]

7.a) Differentiate the working difference between PLA and PAL with example.
b) Explain the basic functionality of CPLD with neat circuit diagrams. [7+8]

8.a) Explain about Chip level Test Techniques.
b) What is the need for testing explain with an example. [8+7]

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