Code No: 54010

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B.Tech II Year II Semester Examinations, May - 2016

SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, ECE, BME, ETM)
Time: 3 hours

Answer any five questions

Max. Marks: 75

Answer any five questions All questions carry equal marks

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	b)	iii) Subtract 743 ₁₀ - 249 ₁₀ by using 2's complement method. Explain the 12-bit Hamming code with one example. [8+7]
X 9 0 X 0 6 0 0 4 0 0 X 0 A 0 A	2.a) b)	Define universal gates and explain its importance used in digital system with example: Realization of four input and gate with two input NOR gate with example. [8+7]
	3.a)	Simplify the following using K-map method. $F(A, B, C, D, E) = \Sigma(0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 2, 31)$
X + + X + 4 + 4 + 4 + 4 + 4 + 4 + 4 + 4	, b)	Implement the following function with NAND gates. $F(x, y, z) = \Sigma(0, 2, 4, 6)$ [8+7]
	4.a)	Define Multiplexer and explain the procedure to implement 32×1 MUX by Using 4×1 Multiplexers.
	b)	Design 4-bit digital comparator with neat sketch and explain its operation. [8+7]
\$ X \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$	· · · · · · · · · · · · · · · · · · ·	Implement $f(A,B,C,D) = \sum_{i=1}^{n} (0,1,4,5,6,7,9,10,12,13,15)$ using PLA and explain its procedure.
	b)	Write the comparisons between PAL, PLA and PROM. [8+7]
6 2 2 3 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	6.a)	What is flip-flop? How can be used in sequential circuit and explain in detail? Design a synchronous modulo-12 counter using NAND gates and JK flip flops. [8+7]
	7.a) b)	Explain the state machine capabilities and limitations in detail. Draw state diagrams of a sequence detector which can Detect 0101. [8+7]
X + + × + × + × + × + × + × + × + × + ×	*** * * * * * * * * * * * * * * * * *	Write short notes on following terms:
		a) ASM charts b) Binary multiplier. [8+7]
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