Code No: 09A40204

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year II Semester Examinations, June-2014
SWITCHING THEORY AND LOGIC DESIGN
(Common to BME, EEE, ECE, ETM)

Time: 3 hours   Max. Marks: 75

Answer any five questions
All questions carry equal marks
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1.a) Convert the following numbers into the corresponding bases.
    i) $(53)_{10}$ = ( )$_2$
    ii) $(231)_8$ = ( )$_{10}$
    iii)$(1101101)2$ =( )$_8$
    iv)$(4D.56)16$=( )$_2$

   b) Encode the following message bits into 7-bit even parity hamming code.
    i) $(1011)_2$
    ii) $(1100)_2$

2.a) Simplify the following Boolean expressions to minimum number of literals using Boolean algebra.
    i) A'C'+ABC+AC'+AB'
    ii) A'B(D'+CD)+B(A+A'CD)

   b) Find the complement of the following functions.
    i) (A'B+CD)E'+E
    ii) XY'+X'Y

3. Simplify the following function using Tabular method
    F(A,B,C,D)= Σ(0,1,2,3,4,6,9,10)+d(7,11,12,13,15).

4.a) Implement the following functions using a decoder.
    F1= Σ(1,3,5,7)
    F2= $\prod$(0,2,5,7)
    F3= Σ(3,4,6,7)

   b) Design a BCD to Excess-3 code converter.

5. Implement the following Boolean functions using PLA
    F1(A,B,C)= Σm(1,2,4,6)
    F2(A,B,C)= Σm(0,1,6,7)
    F3(A,B,C)= Σm(2,6)
    F4(A,B,C)= Σm(1,2,3,5,7).

6.a) Draw the characteristic table of JK flip flop and obtain its characteristic equation.
   b) Realize JK Flip flop using SR Flip flop.

7.a) Discuss the capabilities and limitations of Finite State Machine.
 b) Minimise the following machine using partition method by writing necessary steps involved.

PS	NS,Z	
	x = 0	x = 1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

8.a) What are the basic elements of ASM chart?
 b) Design a binary multiplier and its control logic by drawing ASM chart and realize the same using decoder, MUX and D Flip-Flops.

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