R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations, February - 2014
DIGITAL SYSTEM DESIGN
(Embedded Systems and VLSI Design)

Time: 3 Hours   Max. Marks: 60

Instructions:
  i) Part A is compulsory Question for 20 marks.
  ii) Part B consists of five questions with "either" "or" pattern. The student has to answer any one. However students have to answer five questions from Part B (numbered from 2 to 6)

PART - A
(Answer all sub questions)

5×4 marks = 20

1.a) Discuss in detail about reduction of state tables and state assignments.
  b) Discuss in detail about bridging faults.
  c) Draw the circuit which realizes the function $f(x) = x_1 x_2 + x_3 x_4$ using AND-OR gates using Boolean difference method. Obtain the test set to detect SAO fault on input line x_1 of this circuit.
  d) Discuss the algorithmic steps involved in PODEM.
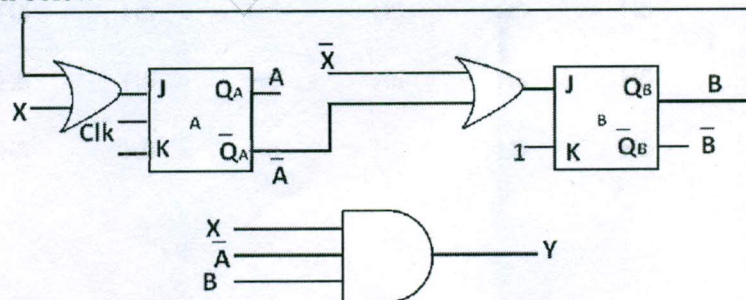 e) Discuss about the circuit test approach.

PART - B

5×8 marks = 40

Answer either "a" or "b" from each question, but not both

2.a) Draw an ASM chart for the control logic of a binary multiplier. Realize the same using MUX, decoder and D-type flip flops.
OR
 b) Derive the state equation, state table and state diagram for the sequential circuit shown below

3.a) i) Explain about various timing issues in any digital system with neat diagrams.
     ii) Highlight the differences between ROM, PLA and PAL.
OR
  b) i) Discuss design of:
         (1) Array multiplier
         (2) Shift and add multiplier.
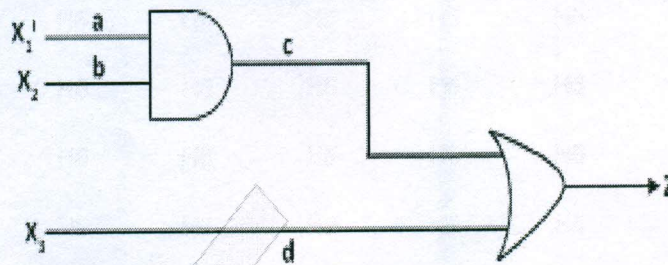   ii) List out the merits and demerits of the above two approaches.

4.a) Apply D-algorithm to detect SAO fault at 'h' in the given circuit and establish the test vectors.
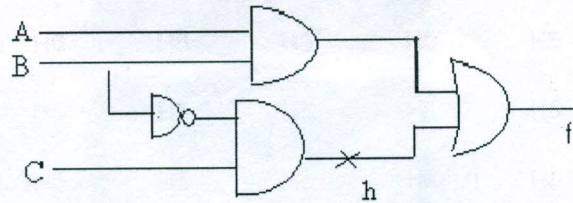
OR

b) Draw the table giving the set of possible single stuck at faults and fault free responses and also construct the fault cover table for the circuit shown below.

5.a) Explain how Kohavi algorithm can be used for detection of faults. Describe based on an example.

OR

b) Describe how signature analysis is done. Highlight its suitability for detecting bridging faults.

6.a) Discuss about the transition check approach.

OR

b) Draw the ASM chart to detect the overlapping sequence 1010 from the incoming bit steam and output 1 for each detection.
   Ex: x: 10101010110-------
        Z: 00010101000-------

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