Code No: 09A60204 R09

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B. Tech III Year II Semester Examinations, May – 2013
Microprocessors and Microcontrollers
(Common to EEE, ECE, EIE, ETM, E.COMP.E, ICE)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) With a neat block diagram explain the architecture of 8086 processor.
b) Explain the following instructions of 8086
i) TEST ii) CMP
iii) XLAT iv) CBW. [8+7]

2.a) What is the purpose of the Instruction Queue of BIU in 8086? Why is the size of the queue limited to 6 Bytes?
b) Explain addressing modes of 8086 with an example. [5+10]

3. An 8086-1 system with 8255 is interfaced at port A address FFF8H and Port C address at FFFEH. 8086-2 system with another 8255 is interfaced at port A address FFF8H and Port C address at FFFEH. Give necessary hardware and software for transferring 10 bytes of data in parallel from 8086-1 to another 8086-2. Assume that both systems run on the same clock rate. [15]

4.a) Explain how to interface Digital-to-Analog Converter (DAC) to 8086 processor. Give the hardware and software for it.
b) Explain type 3 interrupt in 8086. [12+3]

5.a) Draw and explain interrupt acknowledgement cycle of 8086.
b) Explain the mode word format and the command word format of 8251A. [5+10]

6.a) Assume that ROM space of 8051 starting at 250H contains "Hello", write a program to transfer the bytes into RAM locations starting at 40H.
b) Explain the stack operation in 8051 microcontroller and also discuss necessary instructions to access the stack. [9+6]

7.a) List out the steps involved in programming the 8051 to transfer data serially.
b) Write an 8051 program to find Y where $Y = x^2+5$ and x is between 0 and 5. [5+10]

8.a) Explain the salient features of AVR RISC controller with reference to its architecture.
b) Discuss the interrupt structure of RISC controller. [15]

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